Atty. Docket No.: 10001840-1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Roy R. Faget	Group Art Unit:	2124
Serial No.:	09/505,382	Examiner:	Chat C. Do
Filed:	February 16, 2000		

Title: APPARATUS AND METHOD FOR SHARING DATA FET FOR A FOUR-WAY MULTIPLEXER

#9
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Box Non-Fee Amendment
U.S. Patent and Trademark Office
Washington, DC 20231

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REQUEST FOR RECONSIDERATION AFTER FINAL REJECTION

Sir:

In response to the February 4, 2003 Office Action, the following remarks are respectfully submitted:

REMARKS

Claims 1-20 are pending. Reconsideration and allowance of all pending claims is respectfully requested in view of the following remarks.

Claim Rejections Under 35 U.S.C. §102

Claims 1-20 are rejected under 35 U.S.C. §102 (b) over U.S. Patent 5,553,010 to Tanihira et al. (hereafter Tanihira). This rejection is respectfully traversed.

Tanihira is directed to a data shifting circuit capable of an original data width rotation and a double data width rotation. However, Tanihira does not disclose or suggest "wherein each data input uses a single transistor ... the shared data lines interfacing through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates, ... wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" as recited in claim 1.

The Examiner concedes on page 5 of the Office Action that Tanihira does not explicitly show a transistor receiving an input data. The Examiner asserts that "[i]t is known in the art that an AND gates are structured by transistors, and an input received by an AND gate as shown by Tanihira et al. must goes through a transistor as claimed." Applicants respectfully traverse. Prior art multiplexers and their disadvantages are described in the